Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct grammatical errors.

The claims have been amended and new claims added to clarify Applicants disclosed and claimed invention. The amendments find support in the original claims and/or the Specification.

No new matter has been added.

Claim Rejections under 35 USC 103

1. Claims 1-14, and 26 stand rejected under 35 USC Section 103(a) as being unpatentable over Tseng et al. (US, 6,358,800) in view of Chau et al. (US 6, 165,826).

Tseng et al. teach a method of forming a recessed gate structure by first forming a first (silicon oxide) and a second dielectric (silicon nitride) layer on the substrate and then forming an opening in the uppermost (silicon nitride) dielectric layer; then lining the opening with an oxide

liner and then forming a recessed area in the substrate having a width less than the opening width while using the opening as an etching mask. During the process of forming the recessed area a first set of first oxide sidewall spacers is formed from the oxide liner lining the sidewalls of the uppermost dielectric layer (see Abstract; Figures 2C-2F; col 3, lines 24-40).

Tseng et al. then teach forming a second oxide sidewall spacers having a dopant source lining both the opening and recessed area sidewalls (see Figure 2F; col 3, lines 50-67) while exposing the substrate at a bottom portion of the recessed area which is then followed by forming a gate dielectric (col 3, lines 52-55). The dopant source in the second sidewall spacers is later used to form SDE regions (col 4, lines 39-42) by an out-diffusion anneal following removal of the uppermost dielectric (silicon nitride) layer and an ion implantation process (col 4, lines 18-22).

Thus Tseng et al. do not disclose several aspects of Applicants disclosed and claimed invention including:

Tseng et al. do not disclose:

"forming a silicon oxide layer on the silicon substrate;

forming an opening in the silicon oxide layer to include a recessed area **having about the same width as the opening** extending into a thickness portion of the silicon substrate;"

Rather Tseng et al. teach directly away from Applicants disclosed and claimed invention by teaching forming a recessed area **having a width smaller than the opening**.

Tseng et al. also teach away from Applicants disclosed and claimed invention by teaching forming the opening in a silicon nitride uppermost layer rather than a silicon oxide layer.

Tseng et al. additionally do not disclose:

"then lining the opening sidewalls and recessed area sidewalls with at least one dielectric liner **followed by** forming an exposed silicon substrate portion at a bottom portion of the recessed area **having a width smaller than the opening**;"

Rather Tseng et al. teach directly away from Applicants disclosed and claimed invention by teaching **first lining the opening and recessed area followed by forming an exposed area** at the bottom portion of the recessed area.

Tseng et al. also do not disclose:

"then thermally growing a gate oxide over the exposed silicon substrate portion;

Tseng et al. also do not disclose:

"backfilling the opening with polysilicon;

planarizing the polysilicon to the opening level to reveal the silicon oxide layer; and,

selectively removing the silicon oxide layer to form a recessed gate structure."

On the other hand, the fact that Chau et al. discloses that silicon nitride may be used as a sidewall spacers **formed adjacent either side of a gate structure** does not further help Examiner is establishing a *prima facie* case of obviousness.

Even assuming arguendo a proper motivation for combining the teachings of Chau et al. and Tseng et al., such combination does not produce Applicants disclosed and claimed invention.

The structures of Chau et al. and Tseng et al. work by a different principal of operation with respect to each other and with respect to Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention." *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully

solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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